CLAIMS

WHAT IS CLAIMED:

1. A crossbar switch, comprising:

a plurality of input sorting units, each input sorting unit capable of receiving from a respective device an access request to any one of a plurality of physical memory devices;

a plurality of merge and interleave units, each merge and interleave unit capable of arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests and forwarding the selected request for implementation on a respective memory device.

2. The crossbar switch of claim 1, further comprising a plurality of translation circuits and wherein each of the input sorting units receives the access requests through a respective one of the translation circuits.

3. The crossbar switch of claim 2, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

4. The crossbar switch of claim 1, wherein each of the input sorting units includes a buffer and is capable of buffering the access requests from its respective physical memory device.

5. The crossbar switch of claim 4, wherein the buffer is a first-in, first-out queue.

6. The crossbar switch of claim 4, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

7. The crossbar switch of claim 1, wherein each merge and interleave unit includes:

a priority generator for each input sorting unit capable of:

receiving a plurality of characteristics for the access request received by the input sorting unit;

receiving a plurality of operational characteristics; and

generating a composite request priority from the characteristics of the access requests and the operational characteristics;

a priority compare circuit for capable of:

comparing the composite request priorities generated by the priority generators; and

selecting one access request predicated on the comparison of the composite request priorities; and

a request multiplexer controlled by the priority compare circuit to output the selected access request.

8. The crossbar switch of claim 7, wherein the merge and interleave unit further includes:

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

9. The crossbar switch of claim 1, further comprising:

a plurality of read buffers capable of receiving and buffering read data from a respective one of the physical memory devices; and

a plurality of output management units capable of receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

10. The crossbar switch of claim 1, further comprising a plurality of memory interfaces capable of receiving the selected access request from a respective one of the plurality of merge and interleave units and forwarding the selected access request to a respective one of the physical memory devices.

11. A crossbar switch, comprising a plurality of arbitration and select units, each arbitration and select unit including:

a plurality of front ends, each front end comprising:

a translation circuit capable of processing an access request received from a respective device;

an input sorting unit capable of buffering and forwarding the processed access request;

an output management unit capable of receiving read data generated by the access request and forwarding the received read data to the respective device; and

a plurality of back ends, each back end comprising:

a merge and interleave unit capable of arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests, and forwarding the selected request for implementation on a respective memory device; and

a read buffer capable of receiving, buffering, and forwarding read data received from the respective memory device to the output management unit of the front end that issued a previously selected access request that generated the read data.

12. The crossbar switch of claim 11, wherein each back end further comprises a memory interface through which the merge and interleave unit forwards the selected request.

13. The crossbar switch of claim 11, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

14. The crossbar switch of claim 11, wherein each of the input sorting units includes a buffer and is capable of buffering the access requests from its respective physical memory device.

15. The crossbar switch of claim 14, wherein the buffer is a first-in, first-out queue.

16. The crossbar switch of claim 14, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

17. The crossbar switch of claim 11, wherein each merge and interleave unit includes:

a priority generator for each input sorting unit capable of:

receiving a plurality of characteristics for the access request received by the input sorting unit;

receiving a plurality of operational characteristics; and

generating a composite request priority from the characteristics of the access requests and the operational characteristics;

a priority compare circuit capable of:

comparing the composite request priorities generated by the priority generators; and

selecting one access request predicated on the comparison of the composite request priorities; and

a request multiplexer controlled by the priority compare circuit to output the selected access request.

18. The crossbar switch of claim 17, wherein each merge and interleave unit further includes:

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

19. A memory subsystem, comprising:

a plurality of memory devices;

a plurality of devices issuing access requests to the memory devices;

a plurality of input sorting units, each input sorting unit capable of receiving from a respective device an access request to any one of a plurality of physical memory devices;

a plurality of merge and interleave units, each merge and interleave unit capable of arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests and forwarding the selected request for implementation on a respective memory device.

20. The memory subsystem of claim 19, further comprising a plurality of Glue logic units and wherein each of the input sorting units receives the access requests through a respective one of the Glue logic units.

21. The memory subsystem of claim 20, wherein each of the Glue logic units is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

22. The memory subsystem of claim 19, wherein each of the input sorting units includes a buffer and is capable of buffering the access requests from its respective physical memory device.

23. The memory subsystem of claim 22, wherein the buffer is a first-in, first-out queue.

24. The memory subsystem of claim 22, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

25. The memory subsystem of claim 19, wherein each merge and interleave unit includes:

a priority generator for each input sorting unit capable of:

receiving a plurality of characteristics for the access request received by the input sorting unit;

receiving a plurality of operational characteristics; and

generating a composite request priority from the characteristics of the access requests and the operational characteristics;

a priority compare circuit for capable of:

comparing the composite request priorities generated by the priority generators; and

selecting one access request predicated on the comparison of the composite request priorities; and

a request multiplexer controlled by the priority compare circuit to output the selected access request.

26. The memory subsystem of claim 25, wherein the merge and interleave unit further includes:

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

27. The memory subsystem of claim 19, further comprising:

a plurality of read buffers capable of receiving and buffering read data from a respective one of the physical memory devices; and

a plurality of output management units capable of receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

28. The memory subsystem of claim 19, further comprising a plurality of memory interfaces capable of receiving the selected access request from a respective one of the plurality of merge and interleave units and forwarding the selected access request to a respective one of the physical memory devices.

29. The memory subsystem of claim 19, wherein the memory devices include banked DRAMs.

30. The memory subsystem of claim 19, wherein the memory devices comprise at least a portion of a frame buffer.

31. The memory subsystem of claim 19, wherein the devices include pixel processors.

32. A memory subsystem, comprising:

a plurality of memory devices;

a plurality of devices issuing access requests to the memory devices; and

a crossbar switch, comprising a plurality of arbitration and select units, each arbitration and select unit including:

a plurality of front ends, each front end comprising:

a Glue logic unit capable of processing an access request received from a respective device;

an input sorting unit capable of buffering and forwarding the processed access request;

an output management unit capable of receiving read data generated by the access request and forwarding the received read data to the respective device; and

a plurality of back ends, each back end comprising:

a merge and interleave unit capable of arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests, and forwarding the selected request for implementation on a respective memory device; and

a read buffer capable of receiving, buffering, and forwarding read data received from the respective memory device to the output management unit of the front end that issued a previously selected access request that generated the read data.

33. The memory subsystem of claim 32, wherein each back end further comprises a memory interface through which the merge and interleave unit forwards the selected request.

34. The memory subsystem of claim 32, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

35. The memory subsystem of claim 32, wherein each of the input sorting units includes a buffer and is capable of buffering the access requests from its respective physical memory device.

36. The memory subsystem of claim 35, wherein the buffer is a first-in, first-out queue.

37. The memory subsystem of claim 35, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

38. The memory subsystem of claim 32, wherein each merge and interleave unit includes:

a priority generator for each input sorting unit capable of:

receiving a plurality of characteristics for the access request received by the input sorting unit;

receiving a plurality of operational characteristics; and

generating a composite request priority from the characteristics of the access requests and the operational characteristics;

a priority compare circuit for capable of:

comparing the composite request priorities generated by the priority generators; and

selecting one access request predicated on the comparison of the composite request priorities; and

a request multiplexer controlled by the priority compare circuit to output the selected access request.

39. The memory subsystem of claim 38, wherein each merge and interleave unit further includes:

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

40. The memory subsystem of claim 32, wherein the memory devices include banked DRAMs.

41. The memory subsystem of claim 32, wherein the memory devices comprise at least a portion of a frame buffer.

42. The memory subsystem of claim 32, wherein the devices include pixel processors.

43. A method for accessing a shared memory, the method comprising:
receiving a plurality of access requests from a plurality of devices, each access request being received by a respective input sorting unit associated with the respective one of the devices issuing the respective access request;
forwarding a plurality of received access requests to a plurality of merge and interleave units, each merge and interleave unit being associated with a respective one of a plurality of memory devices;
receiving at one of the merge and interleave units a plurality of forwarded access requests;
dynamically selecting a respective one from among forwarded access requests; and
forwarding the selected access request to a respective one among a plurality of memory devices associated with the merge and interleave unit.

44. The method of claim 43, further comprising at least one of:
issuing the plurality of access requests;
implementing the selected access request on the respective memory device; and
returning read data from the respective memory device responsive to the selected access request.

45. The method of claim 44, wherein returning the read data includes:
buffering the read data in a read buffer associated with the respective memory device;
forwarding the read data to an output management unit associated with a respective one of the devices that issued a previously selected access request resulting in the return of the read data.

46. The method of claim 43, further comprising, for each access request:
processing the access request; and
forwarding the processed access request to the respective input sorting unit.

47. The method of claim 46, wherein processing the access request includes:
receiving an opcode and a virtual address from the respective device;
translating the opcode to determine whether the access request is a read or a write;
mapping the virtual address into a physical address; and
forwarding the translated opcode and mapped physical address to the respective input sorting unit.

48. The method of claim 43, wherein receiving the access requests includes receiving a plurality of characteristics for the access requests.

49. The method of claim 48, wherein dynamically selecting the particular access request includes:

ascertaining a plurality of operational characteristics;

assigning a weight factor to each characteristic of the access requests;

assigning a weight factor to each operational characteristic;

obtaining a composite request priority for each access request from the access request's respective assigned weight factors;

comparing the composite request priorities of the access requests; and

selecting the particular access requests predicated on the comparison.

50. The method of claim 49, wherein obtaining the composite request priority for each access request includes summing the assigned weight factors.

51. The method of claim 49, wherein selecting one of the access requests predicated on the comparison includes selecting the access request with the highest composite priority.

52. The method of claim 49, further comprising programming the values of the assigned weight factors before they are assigned.

53. The method of claim 49, further comprising increasing the composite request priority of each access request not selected or decreasing the composite request priority of the selected request.

54. The method of claim 43, wherein forwarding the selected access request to the respective memory device includes forwarding the selected access request to a memory interface.

55. A crossbar switch, comprising a plurality of arbitration and select units, each arbitration and select unit including:

a plurality of front ends, each front end further including an input sorting unit capable of receiving from a respective device an access request to any one of a plurality of physical memory devices;

a plurality of back ends, each back end further including merge and interleave unit capable of arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests and forwarding the selected request for implementation on a respective memory device

56. The crossbar switch of claim 55, wherein each front end further comprises a Glue logic unit and wherein each of the input sorting units receives the access requests through a respective one of the Glue logic units.

57. The crossbar switch of claim 56, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

58. The crossbar switch of claim 55, wherein each of the input sorting units includes a buffer and is capable of buffering the access requests from its respective physical memory device.

59. The crossbar switch of claim 58, wherein the buffer is a first-in, first-out queue.

60. The crossbar switch of claim 58, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

61. The crossbar switch of claim 55, wherein each merge and interleave unit includes:

a priority generator for each input sorting unit capable of:

receiving a plurality of characteristics for the access request received by the input sorting unit;

receiving a plurality of operational characteristics; and

generating a composite request priority form the characteristics of the access requests and the operational characteristics;

a priority compare circuit for capable of:

comparing the composite request priorities generated by the priority generators; and

selecting one access request predicated on the comparison of the composite request priorities; and

a request multiplexer controlled by the priority compare circuit to output the selected access request.

62. The crossbar switch of claim 61, wherein each merge and interleave unit further includes:

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

63. The crossbar switch of claim 55, wherein:

each back end further includes a read buffer capable of receiving and buffering read data from a respective one of the physical memory devices; and

each front end further includes an output management unit capable of receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

64. The crossbar switch of claim 55, wherein each back end further comprises a memory interface capable of receiving the selected access request from the merge and interleave unit and forwarding the selected access request to a respective one of the physical memory devices.

65. A crossbar switch, comprising a plurality of arbitration and select units, each arbitration and select unit including:

a plurality of front ends, each front end comprising:

means for processing an access request received from a respective device;

means for buffering and forwarding the processed access request;

means for receiving read data generated by the access request and forwarding the received read data to the respective device; and

a plurality of back ends, each back end comprising:

means for arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests, and forwarding the selected request for implementation on a respective memory device; and

means for receiving, buffering, and forwarding read data received from the respective memory device to the output management unit of the front end that issued a previously selected access request that generated the read data.

66. The crossbar switch of claim 65, wherein each back end further comprises a memory interface through which the merge and interleave unit forwards the selected request.

67. The crossbar switch of claim 65, wherein each processing means is further capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

68. The crossbar switch of claim 65, wherein each of the processed access request buffering means includes a buffer and is capable of buffering the access requests from its respective physical memory device.

69. The crossbar switch of claim 68, wherein the buffer is a first-in, first-out queue.

70. The crossbar switch of claim 68, wherein each of the processed access request buffering means is capable of stalling its respective device when its buffer is full.

71. The crossbar switch of claim 65, wherein each arbitration and selection means includes:

means for receiving a plurality of characteristics for the access request received by the input sorting unit, receiving a plurality of operational characteristics, and generating a composite request priority from the characteristics of the access requests and the operational characteristics;

means for comparing the composite request priorities generated by the priority generators, and selecting one access request predicated on the comparison of the composite request priorities; and

means for multiplexing signals, the multiplexing means being controlled by the comparing means to output the selected access request.

72. The crossbar switch of claim 71, wherein each arbitration and selection means further includes:

means for storing programmable weights;

a decode unit receiving the selected request from the multiplexing means to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the storage means; and

means for combining register read data with request data for output.

73. The crossbar switch of claim 65, wherein:

each back end further includes means for receiving and buffering read data from a respective one of the physical memory devices; and

each front end further includes means for receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

74. A memory subsystem, comprising:

a plurality of memory devices;

a plurality of devices issuing access requests to the memory devices;

means for receiving from a respective device an access request to any one of a plurality of physical memory devices;

means for arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests and forwarding the selected request for implementation on a respective memory device.

75. The memory subsystem of claim 74, wherein:

the receiving means includes a plurality of input sorting units; or

the arbitration and selection means includes a plurality of merge and interleave units.

76. The memory subsystem of claim 75, wherein the receiving means further comprises a plurality of Glue logic units and wherein each of the input sorting units receives the access requests through a respective one of the Glue logic units.

77. The memory subsystem of claim 76, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

78. The memory subsystem of claim 74, wherein receiving means furthermore buffers the access requests.

79. The memory subsystem of claim 78, wherein the receiving means includes a first-in, first-out queue for buffering the access requests.

80. The memory subsystem of claim 78, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

81. The memory subsystem of claim 74, wherein the arbitration and selection means includes:

a priority generator for each input sorting unit capable of:

receiving a plurality of characteristics for the access request received by the input sorting unit;

receiving a plurality of operational characteristics; and

generating a composite request priority from the characteristics of the access requests and the operational characteristics;

a priority compare circuit for capable of:

comparing the composite request priorities generated by the priority generators; and

selecting one access request predicated on the comparison of the composite request priorities; and

a request multiplexer controlled by the priority compare circuit to output the selected access request.

82. The memory subsystem of claim 81, wherein the merge and interleave unit further includes:

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

83. The memory subsystem of claim 74, further comprising:

means for receiving and buffering read data from a respective one of the physical memory devices; and

means for receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

84. The memory subsystem of claim 83, wherein:

the receiving and buffering means includes a plurality of read buffers; or

the receiving and forwarding data includes a plurality of output management units.

85. The memory subsystem of claim 74, further comprising means for receiving the selected access request from the arbitration and selection means and forwarding the selected access request to a respective one of the physical memory devices.

86. The memory subsystem of claim 85, wherein the receiving and forwarding means comprises a plurality of memory interfaces.

87. The memory subsystem of claim 74, wherein the memory devices include banked DRAMs.

88. The memory subsystem of claim 74, wherein the memory devices comprise at least a portion of a frame buffer.

89. The memory subsystem of claim 74, wherein the devices include pixel processors.

90. A crossbar switch, comprising:

means for receiving a plurality of access requests from a plurality of devices, each access request being received by a respective input sorting unit associated with the respective one of the devices issuing the respective access request;

means for forwarding a plurality of received access requests to a plurality of merge and interleave units, each merge and interleave unit being associated with a respective one of a plurality of memory devices;

means for receiving at one of the merge and interleave units a plurality of forwarded access requests;

means for dynamically selecting a respective one from among forwarded access requests; and

means for forwarding the selected access request to a respective one among a plurality of memory devices associated with the merge and interleave unit.

91. The crossbar switch of claim 90, further comprising at least one of:

means for issuing the plurality of access requests;

means for implementing the selected access request on the respective memory device; and

means for returning read data from the respective memory device responsive to the selected access request.

92. The crossbar switch of claim 91, wherein the means for returning the read data includes:

means for buffering the read data in a read buffer associated with the respective memory device;

means for forwarding the read data to an output management unit associated with a respective one of the devices that issued a previously selected access request resulting in the return of the read data.

93. The crossbar switch of claim 90, further comprising, for each access request:

means for processing the access request; and

means for forwarding the processed access request to the respective input sorting unit.

94. The crossbar switch of claim 93, wherein the means for processing the access request includes:

means for receiving an opcode and a virtual address from the respective device;

means for translating the opcode to determine whether the access request is a read or a write;

means for mapping the virtual address into a physical address; and

means for forwarding the translated opcode and mapped physical address to the respective input sorting unit.

95. The crossbar switch of claim 90, wherein the means for receiving the access requests includes means for receiving a plurality of characteristics for the access requests.

96. The method of claim 95, wherein the means for dynamically selecting the particular access request includes:

ascertaining a plurality of operational characteristics;

assigning a weight factor to each characteristic of the access requests;

assigning a weight factor to each operational characteristic;

obtaining a composite request priority for each access request from the access request's respective assigned weight factors;

comparing the composite request priorities of the access requests; and

selecting the particular access requests predicated on the comparison.

97. The crossbar switch of claim 96, wherein the means for obtaining the composite request priority for each access request includes means for summing the assigned weight factors.

98. The crossbar switch of claim 96, wherein the means for selecting one of the access requests predicated on the comparison includes means for selecting the access request with the highest composite priority.

99. The crossbar switch of claim 96, further comprising means for programming the values of the assigned weight factors before they are assigned.

100. The crossbar switch of claim 96, further comprising means for increasing the composite request priority of each access request not selected or decreasing the composite request priority of the selected request.

101. The crossbar switch of claim 90, wherein the means for forwarding the selected access request to the respective memory device includes forwarding the selected access request to a memory interface.

102. A crossbar switch, comprising:

means for receiving from a respective device an access request to any one of a plurality of physical memory devices;

means for arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests and forwarding the selected request for implementation on a respective memory device.

103. The crossbar switch of claim 102, wherein:

the receiving means includes a plurality of input sorting units; or

the arbitration and selection means includes a plurality of merge and interleave units.

104. The crossbar switch of claim 103, wherein the receiving means further comprises a plurality of translation circuits and wherein each of the input sorting units receives the access requests through a respective one of the Translation circuits.

105. The crossbar switch of claim 104, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

106. The crossbar switch of claim 102, wherein receiving means furthermore buffers the access requests.

107. The crossbar switch of claim 106, wherein the receiving means includes a first-in, first-out queue for buffering the access requests.

108. The crossbar switch of claim 106, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

109. The crossbar switch of claim 102, wherein the arbitration and selection means includes:

a priority generator for each input sorting unit capable of:

receiving a plurality of characteristics for the access request received by the input sorting unit;

receiving a plurality of operational characteristics; and

generating a composite request priority from the characteristics of the access requests and the operational characteristics;

a priority compare circuit for capable of:

comparing the composite request priorities generated by the priority generators; and

selecting one access request predicated on the comparison of the composite request priorities; and

a request multiplexer controlled by the priority compare circuit to output the selected access request.

110. The crossbar switch of claim 109, wherein the merge and interleave unit further includes:

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

111. The crossbar switch of claim 102, further comprising:

means for receiving and buffering read data from a respective one of the physical memory devices; and

means for receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

112. The crossbar switch of claim 111, wherein:

the receiving and buffering means includes a plurality of read buffers; or

the receiving and forwarding data includes a plurality of output management units.

113. The crossbar switch of claim 102, further comprising means for receiving the selected access request from the arbitration and selection means and forwarding the selected access request to a respective one of the physical memory devices.

114. The crossbar switch of claim 113, wherein the receiving and forwarding means comprises a plurality of memory interfaces.

115. A computing device, comprising

a plurality of memory devices;

a plurality of devices issuing access requests to the memory devices;

a plurality of input sorting units, each input sorting unit capable of receiving from a respective device an access request to any one of a plurality of physical memory devices;

a plurality of merge and interleave units, each merge and interleave unit capable of arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests and forwarding the selected request for implementation on a respective memory device.

116. The computing device of claim 115, further comprising a plurality of translation circuits and wherein each of the input sorting units receives the access requests through a respective one of the translation circuits.

117. The computing device of claim 116, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

118. The computing device of claim 115, wherein each of the input sorting units includes a buffer and is capable of buffering the access requests from its respective physical memory device.

119. The computing device of claim 118, wherein the buffer is a first-in, first-out queue.

120. The computing device of claim 118, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

121. The computing device of claim 115, wherein each merge and interleave unit includes:

a priority generator for each input sorting unit capable of:

receiving a plurality of characteristics for the access request received by the input sorting unit;

receiving a plurality of operational characteristics; and

generating a composite request priority from the characteristics of the access requests and the operational characteristics;

a priority compare circuit for capable of:

comparing the composite request priorities generated by the priority generators; and

selecting one access request predicated on the comparison of the composite request priorities; and

a request multiplexer controlled by the priority compare circuit to output the selected access request.

122. The computing device of claim 121, wherein the merge and interleave unit further includes:

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

123. The computing device of claim 115, further comprising:

a plurality of read buffers capable of receiving and buffering read data from a respective one of the physical memory devices; and

a plurality of output management units capable of receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

124. The computing device of claim 115, further comprising a plurality of memory interfaces capable of receiving the selected access request from a respective one of the plurality of merge and interleave units and forwarding the selected access request to a respective one of the physical memory devices.

125. The computing device of claim 115, wherein the memory devices include banked DRAMs.

126. The computing device of claim 115 wherein the memory devices comprise at least a portion of a frame buffer.

127. The computing device of claim 115, wherein the devices include pixel processors.

128. A computing device, comprising:

a plurality of memory devices;

a plurality of devices issuing access requests to the memory devices; and

a crossbar switch, comprising a plurality of arbitration and select units, each arbitration and select unit including:

a plurality of front ends, each front end comprising:

a translation circuit capable of processing an access request received from a respective device;

an input sorting unit capable of buffering and forwarding the processed access request;

an output management unit capable of receiving read data generated by the access request and forwarding the received read data to the respective device; and

a plurality of back ends, each back end comprising:

a merge and interleave unit capable of arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests, and forwarding the selected request for implementation on a respective memory device; and

a read buffer capable of receiving, buffering, and forwarding read data received from the respective memory device to the output

management unit of the front end that issued a previously selected access request that generated the read data.

129. The computing device of claim 128, wherein each back end further comprises a memory interface through which the merge and interleave unit forwards the selected request.

130. The computing device of claim 128, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

131. The computing device of claim 128, wherein each of the input sorting units includes a buffer and is capable of buffering the access requests from its respective physical memory device.

132. The computing device of claim 131, wherein the buffer is a first-in, first-out queue.

133. The computing device of claim 131, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

134. The computing device of claim 128, wherein each merge and interleave unit includes:

a priority generator for each input sorting unit capable of:

receiving a plurality of characteristics for the access request received by the input sorting unit;

receiving a plurality of operational characteristics; and

generating a composite request priority from the characteristics of the access requests and the operational characteristics;

a priority compare circuit for capable of:

comparing the composite request priorities generated by the priority generators; and

selecting one access request predicated on the comparison of the composite request priorities; and

a request multiplexer controlled by the priority compare circuit to output the selected access request.

135. The computing device of claim 134, wherein each merge and interleave unit further includes:

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

136. The computing device of claim 128, wherein the memory devices include banked DRAMs.

137. The computing device of claim 128, wherein the memory devices comprise at least a portion of a frame buffer.

138. The computing device of claim 128, wherein the devices include pixel processors.

139. A computing device, comprising:

a plurality of memory devices;

a plurality of devices issuing access requests to the memory devices;

means for receiving from a respective device an access request to any one of a plurality of physical memory devices;

means for arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests and forwarding the selected request for implementation on a respective memory device.

140. The computing device of claim 139, wherein:

the receiving means includes a plurality of input sorting units; or

the arbitration and selection means includes a plurality of merge and interleave units.

141. The computing device of claim 140, wherein the receiving means further comprises a plurality of translation circuits and wherein each of the input sorting units receives the access requests through a respective one of the translation circuits.

142. The computing device of claim 141, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

143. The computing device of claim 139, wherein receiving means furthermore buffers the access requests.

144. The computing device of claim 143, wherein the receiving means includes a first-in, first-out queue for buffering the access requests.

145. The computing device of claim 143, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

146. The computing device of claim 139, wherein the arbitration and selection means includes:

a priority generator for each input sorting unit capable of:

receiving a plurality of characteristics for the access request received by the input sorting unit;

receiving a plurality of operational characteristics; and

generating a composite request priority from the characteristics of the access requests and the operational characteristics;

a priority compare circuit for capable of:

comparing the composite request priorities generated by the priority generators; and

selecting one access request predicated on the comparison of the composite request priorities; and

a request multiplexer controlled by the priority compare circuit to output the selected access request.

147. The computing device of claim 146, wherein the merge and interleave unit further includes:

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

148. The computing device of claim 139, further comprising:

means for receiving and buffering read data from a respective one of the physical memory devices; and

means for receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

149. The computing device of claim 148, wherein:

the receiving and buffering means includes a plurality of read buffers; or

the receiving and forwarding data includes a plurality of output management units.

150. The computing device of claim 139, further comprising means for receiving the selected access request from the arbitration and selection means and forwarding the selected access request to a respective one of the physical memory devices.

151. The computing device of claim 150, wherein the receiving and forwarding means comprises a plurality of memory interfaces.

152. The computing device of claim 139, wherein the memory devices include banked DRAMs.

153. The computing device of claim 139, wherein the memory devices comprise at least a portion of a frame buffer.

154. The computing device of claim 139, wherein the devices include pixel processors.